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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,243	03/28/2001	Terry L. Kendall	42390P10070	3769

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA. 90025

EXAMINER

PORTKA, GARY J

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 06/16/2003

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/820,243

Applicant(s)
Kendall

Examiner
Gary J. Portka

Art Unit
2188



— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Apr 16, 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 21-24 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 21-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

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DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 4, 2003 has been entered.

2. Claims 1 and 6 have been amended. Claims 1-9 and 21-24 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor et al., U.S. Patent 6,263,398 B1.

5. As to claims 1-3, Taylor discloses the recited memory with cache, integrated, and flash (see Abstract, Figure 1, and column 3 lines 7-35). The additional limitation of simultaneously containing multiple addresses is also disclosed since each row stored in the cache is made up of multiple column addresses (which are shown separately in Figures 4-7). See Figure 1, and column 4 line 58 to column 5 line 11.

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6. Claims 1-2, 6-7, and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto, U.S. Patent 6,288,923 B1.

7. As to claims 1-2, Sakamoto discloses the recited memory with cache, integrated (see Abstract, Figure 2, column 1 line 57 to column 2 line 8). The additional limitation of simultaneously containing multiple addresses is also disclosed since the data array 26 of cache 20 (Figure 2) stores multiple addresses (see registers of Figure 4).

8. As to claims 6-7, Sakamoto discloses the recited memory with cache, integrated (see Abstract, Figure 2, column 1 line 57 to column 2 line 8). The additional limitation of storing non-consecutive addresses in adjacent locations in the cache is also disclosed since the data array 26 of cache 20 (Figure 2) is accessed using tag array 21, from which hit/miss must be determined (see col. 4 lines 35-39). Since any memory data may hit or miss in the cache, clearly the registers of the data array may contain different memory addresses, and therefore store non-consecutive adjacently (see Figure 4).

9. As to claims 21 and 23, Sakamoto discloses quadwords to the extent recited. See Figures 6-10, where data is output in groups of four registers. Multiple and non-consecutive quadwords are stored simultaneously in the register array shown in Figure 4.

10. As to claims 22 and 24, Sakamoto discloses cache 20 having address cache 21 and data cache 26 (see Figure 2).

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Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, or alternatively over Taylor et al., U.S. Patent 6,263,398 B1.

13. As to claim 5, neither Sakamoto nor Taylor disclose integrating the memory and cache with the processor. However, each teaches benefits of integrating in general (may lower costs and improve performance); such benefits are notoriously well known in the art and likewise well known to be scalable. Examiner takes Official Notice that an artisan would have known that integrating memory and cache with processor might provide like benefits and would have thus desired to do so. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate memory, cache, and processor, because integration is scalable and the benefits thereof were well known.

14. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of Motomura, U.S. Patent 6,347,055 B1; or alternatively over Taylor et al., U.S. Patent 6,263,398 B1, in view of Motomura, U.S. Patent 6,347,055 B1.

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15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of Motomura, U.S. Patent 6,347,055 B1.

16. As to claims 4 and 9, neither Sakamoto nor Taylor disclose the cache holding no more than sixteen addresses. However, an artisan would have recognized the trade-offs between cache size and chip real estate. Motomura teaches an analogous memory integrated with line buffer circuit which holds no more than sixteen addresses (see Figures 1, 5). The line buffers are analogous to a cache because they are used to improve performance, and include cache characteristics including hit/miss and associativity (see column 1 lines 10-12, and column 8 lines 1-14). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a cache holding no more than sixteen addresses, because this was a known configuration to achieve a desired price-performance compromise.

17. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of Taylor et al., U.S. Patent 6,263,398 B1.

18. As to claim 8, Sakamoto does not disclose a flash memory. However, Taylor teaches that it is beneficial to integrate a cache onto a flash memory. An artisan would have been motivated to use flash memory because it is non-volatile, and because it was known to benefit from on-chip caching. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use flash, because it was known to benefit from on-chip caching, and is non-volatile.

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Response to Arguments

19. Applicant's arguments filed March 4, 2003 have been fully considered but they are not persuasive.

Applicants argue that Taylor is limited to storing a single address at a time, the page address. Examiner disagrees. As described above, one row is made up of multiple columns, each with a column address derived from the address input at 16, and selected from cache 14 by column decoder 26, Figure 1. See also Figure 2 through 6, where even after a row hit in the cache is determined, the column address is required to access the data.

Conclusion

20. Any inquiry concerning this communication from the examiner should be directed to Gary J. Portka at telephone number (703) 305-4033. The examiner can normally be reached on weekdays from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks, can be reached at (703) 308-1756.

Any response to this action should be mailed to (or faxed as provided below):

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (Receptionist).

The fax phone number for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final communications)

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(703) 746-7239 (Official communications)

(703) 746-7240 (Status inquiries, draft communications)

Any inquiry of a general nature relating to this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 305-3900.

Gary J. Portka

Primary Examiner

June 13, 2003

A handwritten signature in cursive script, reading "Gary J. Portka".